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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,956	01/05/2004	Shinichi Ukon	8044-1029	2053

466 7590 12/31/2007

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EXAMINER	
RIVAS, SALVADOR E	
ART UNIT	**PAPER NUMBER**
2619	

MAIL DATE	DELIVERY MODE
12/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,956	UKON ET AL.	
	Examiner	Art Unit	
	Salvador E. Rivas	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/05/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement submitted on January 5, 2004 been considered by the Examiner and made of record in the application file.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7-9 are rejec ted under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling to claim 7 due to a lack of a second route. In claim 7 (page 55 Lines 23-25) a second link is needed in case the original communication link suffers a failure thereby allowing for communication to occur between a source and destination which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188

USPQ 356 (CCPA 1976). On claim 7 (page 55 Lines 23-25) the applicant states that once a fault notification has been received by the termination node, said termination node sends "... back switching instruction data representing port switching through the clock supply route;" How can this be possible since only one clock supply route or link is being used to transmit back a fault notification and this clock supply route has been identified as faulty, therefore no signal would be able to be transmitted back to the source.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Puppa et al. (US Patent # 7,092,361 B2),** in view of **Murata (US Patent # 7,177,327 B2),** and further in view of **Storr (U.S. Patent # 7,072,302 B1)**.

Regarding **claim 1**, Murata teaches a synchronous clock supply system (Fig. 13) comprising: and a termination node which is positioned in a downstream side (Fig.13 @ 17) of the clock supply route farther than the relay node from a synchronous clock sending source (Fig.13 @ 16) used to synchronize the nodes in the network. However, Murata fails to teach at least one relay node which is positioned in a clock supply route formed by coupling arbitrary virtual paths for nodes in a network; and finally receives the synchronous clock via a predetermined port, the relay node having fault detection means for, when no synchronous clock is supplied in a downstream direction from an upstream side of the clock supply route due to a fault in the virtual path, detecting that no synchronous clock is supplied, fault notification data transmission means for, when said fault detection means detects the fault, sending fault notification data representing occurrence of the fault to the downstream side of the clock supply route, and first port switching means for, when switching instruction data designating switching to another

port for supply of the synchronous clock is sent in the upstream side from the downstream side of the clock supply route, switching a port for receiving the synchronous clock to the port, and the termination node having second port switching means for, when another port is connected to the sending source via another virtual path and the fault notification data is sent from the relay node, performing port switching for supplying the synchronous clock from the predetermined port to said another port, and port switching instruction means for, when said port switching means performs port switching, sending switching instruction data which instructs the upstream side of the clock supply route to switch the port to said another port for supply of the synchronous clock.

Puppa et al. teach a system and method for "... notifying a first communication network of a fault related to a second communication network ..." (Column 1 Lines 33-35). Also, Puppa et al. teach at least one relay node (read as an ATM/MPLS edge router (Fig.4 @ 122 and Fig.6)) which is positioned in a clock supply route formed by coupling arbitrary virtual paths for nodes in a network; and finally receives the synchronous clock via a predetermined port ("... ATM/MPLS edge switch 122 comprises an ATM card 400, a fabric card 402, an MLPS card 404, at least one ATM port 406, at least one MPLS port 408, two fabric ports 410 and 412, a control card (not shown in this figure) and two I/O cards (not shown)." Column 4 Lines 46-50), the relay node (read as an ATM/MPLS edge router (Fig.4 @ 122 and Fig.6)) having fault detection means for (read as an OAM Protocol), when no synchronous clock is supplied in a downstream direction from an upstream side of the clock supply route due to a fault

in the virtual path, detecting that no synchronous clock is supplied ("... ATM/MPLS edge switch 122 is capable of indicating a failure in MPLS network 104 to ATM network 102 by monitoring tunnel 204 and by messaging to ATM network 102 the arrival of MPLS OAM frames." Column 5 Lines 15-18), fault notification data transmission means for (read as an OAM Protocol), when said fault detection means detects the fault, sending fault notification data representing occurrence of the fault to the downstream side of the clock supply route ("Upon a failure of an element in this routing path, for example communications link 108, an ATM OAM cell is generated and transmitted over ATM network 102(1) to inform ATM edge switches 110(1) and 110(3) of the failure."(Column 5 Lines 26-30). It would have been obvious to a person of ordinary skill in the art to combine the ATM/MPLS edge router of Puppa et al. with the system that provides synchronous clock signals of Murata for the purpose of recognizing and alerting a network element of failure on a communication link. The motivation being to efficiently having a data transmission apparatus regulate the transmission of ATM cells in an ATM network.

However, Murata and Puppa et al. fails to teach where first port switching means for, when switching instruction data designating switching to another port for supply of the synchronous clock is sent in the upstream side from the downstream side of the clock supply route, switching a port for receiving the synchronous clock to the port, and the termination node having second port switching means for, when another port is connected to the sending source via another virtual path and the fault notification data (read as an ATM AIS cell) is sent from the relay node, performing port switching for

supplying the synchronous clock from the predetermined port to said another port, and port switching instruction means for, when said port switching means performs port switching, sending switching instruction data which instructs the upstream side of the clock supply route to switch the port to said another port for supply of the synchronous clock. Storr teaches a data traffic transmission management in "... an asynchronous mode network ... using forward and backward resource management cells." (Column 1 Lines 42-44) Also, Storr teaches a first port switching means for (read a switching fabric (Fig.3 @ 302)), when switching instruction data designating switching to another port for supply of the synchronous clock is sent in the upstream side from the downstream side of the clock supply route, switching a port for receiving the synchronous clock to the port ("ATM cells sent to or from a port **310**, **320**, or **330** are processed by port circuitry and may be switched among ports by switching fabric **302** ." Column 6 Lines 61-63), and the termination node having second port switching means for (Fig.3 @ 302), when another port is connected to the sending source via another virtual path ("... receiving a control cell on a virtual channel from a source node, generating a management event upon receipt of the control cell, and processing the management even to compute resource management data. Upon the subsequent receipt of a control cell on a virtual channel from a destination node, the control cell from the destination node is modified using the computed resource management data and transmitted over the first virtual channel toward the source node." Column 1 Lines 55-59) and the fault notification data (read as an ATM AIS cell) is sent from the relay node (Fig.3 @ 300 provides "resource management services" (Column 6 Lines 58-59)), performing port switching (Fig.3 @

302) for supplying the synchronous clock from the predetermined port to said another port, and port switching instruction means for, when said port switching means performs port switching, sending switching instruction data which instructs the upstream side of the clock supply route to switch the port to said another port for supply of the synchronous clock ("ATM cells sent to or from a port **310** , **320** , or **330** are processed by port circuitry and may be switched among ports by switching fabric **302** ." Column 6 Lines 61-63). It would have been obvious to a person of ordinary skill in the art to combine the ATM switch of Storr with ATM/MPLS edge router of Puppa et al. and the system that provides synchronous clock signals of Murata for the purpose of data traffic management using forward and backward resource management cells. The motivation being to efficiently having a data transmission apparatus regulate the transmission of ATM cells in an ATM network.

Regarding **claim 2**, and **as applied to claim 1 above**, Murata, as modified by Puppa et al. and Storr, teaches a system further comprising clock sending means (Fig. 4 @ 6) for sending the synchronous clock to the clock supply route (Fig.4 @ 1).

Regarding **claim 3**, and **as applied to claim 1 above**, Murata, as modified by Puppa et al. and Storr, teaches a system wherein the clock supply route includes a plurality of clock supply routes, the synchronous clock is sent to the respective clock supply routes, the relay node (Fig.4) includes relay nodes for the respective clock supply routes (Fig.4 @ 7, "... UNI service control unit **7** generates and suspends a clock pulse according to user conditions and circuit conditions." Column 4 Lines 62-64), and the termination node (Fig.4) includes termination nodes for the respective clock supply

routes (Fig.4 @ 9, "... user condition storing unit **9** stores user information, such as a terminal specification and a contracted circuit speed." Column 5 Lines 10-12).

Regarding **claim 4**, and **as applied to claim 1 above**, Murata teaches a system wherein the synchronous clock includes a synchronous clock which is obtained by extracting a frequency component from a signal used for communication between the nodes and has a unit time as a period (Fig.4 @ 6, "... reference clock generating unit **6** extracts a reference clock signal from the terminal, extracts an external clock signal, generates and supplies a reference clock, and so on. The reference clock generating unit **6** stores information relative to the maximum transmission speed of a circuit to be used, and supplies the maximum transmission speed clock, i.e., the reference clock, to each block by a clock of its own or an externally inputted clock." Column 4 Lines 54-61). However, Murata fails to teach said fault notification data transmission means sends the fault notification data as part of an ATM cell, when the switching instruction data is sent as part of an ATM cell from the upstream direction, said first port switching means switches the port for receiving the synchronous clock to a port which receives the switching instruction data, when the fault notification data is sent as part of the ATM cell from the relay node, said second port switching means switches the port for supplying the synchronous clock from the predetermined port to said another port, and said port switching instruction means sends the switching instruction data as part of an ATM cell.

Puppa et al. teach a system and method for "... notifying a first communication network of a fault related to a second communication network ..." (Column 1 Lines 33-35). Also, Puppa et al. teach an ATM/MPLS edge router (Fig.4 @ 122 and Fig.6) having

said fault notification data transmission means sends the fault notification data as part of an ATM cell, when the switching instruction data is sent as part of an ATM cell from the upstream direction, ("Upon a failure of an element in this routing path, for example communications link 108, an ATM OAM cell is generated and transmitted over ATM network 102(1) to inform ATM edge switches 110(1) and 110(3) of the failure."(Column 5 Lines 26-30). It would have been obvious to a person of ordinary skill in the art to combine the ATM/MPLS edge router of Puppa et al. with the system that provides synchronous clock signals of Murata for the purpose of recognizing and alerting a network element of failure on a communication link. The motivation being to efficiently having a data transmission apparatus regulate the transmission of ATM cells in an ATM network.

However, Murata and Puppa et al. fails to teach said first port switching means switches the port for receiving the synchronous clock to a port which receives the switching instruction data, when the fault notification data is sent as part of the ATM cell from the relay node, said second port switching means switches the port for supplying the synchronous clock from the predetermined port to said another port, and said port switching instruction means sends the switching instruction data as part of an ATM cell. Storr teaches a data traffic transmission management in "... an asynchronous mode network ... using forward and backward resource management cells." (Column 1 Lines 42-44) Also, Storr teaches said first port switching means (read as switch fabric) switches the port for receiving the synchronous clock to a port which receives the switching instruction data , when the fault notification data is sent as part of the ATM cell

from the relay node ("... receiving a control cell on a virtual channel from a source node, generating a management event upon receipt of the control cell, and processing the management even to compute resource management data. Upon the subsequent receipt of a control cell on a virtual channel from a destination node, the control cell from the destination node is modified using the computed resource management data and transmitted over the first virtual channel toward the source node." Column 1 Lines 55-59), said second port switching means switches the port for supplying the synchronous clock from the predetermined port to said another port, and said port switching instruction means sends the switching instruction data as part of an ATM cell ("ATM cells sent to or from a port **310**, **320**, or **330** are processed by port circuitry and may be switched among ports by switching fabric **302**." Column 6 Lines 61-63). It would have been obvious to a person of ordinary skill in the art to combine the ATM switch of Storr with ATM/MPLS edge router of Puppa et al. and the system that provides synchronous clock signals of Murata for the purpose of data traffic management using forward and backward resource management cells. The motivation being to efficiently having a data transmission apparatus regulate the transmission of ATM cells in an ATM network.

Regarding **claim 5**, and **as applied to claim 4 above**, Murata, as modified by Puppa et al. and Storr, teaches teach a system wherein the clock supply route includes a plurality of clock supply routes, the synchronous clock is sent to the respective clock supply routes, the relay node (Fig.4) includes relay nodes (Fig.4 @ 9) for the respective clock supply routes (Fig.4 @ 7, "... UNI service control unit **7** generates and suspends a clock pulse according to user conditions and circuit conditions." Column 4 Lines 62-64),

and the termination node (Fig.4) includes termination nodes for the respective clock supply routes ("... user condition storing unit **9** stores user information, such as a terminal specification and a contracted circuit speed." Column 5 Lines 10-12).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Puppa et al. (US Patent # 7,092,361 B2),** in view of **Murata (US Patent # 7,177,327 B2),** and further in view of **Storr (U.S. Patent # 7,072,302 B1) and Puleston (U.S. Patent # 2002/0181480 A1)**.

Regarding **claim 6**, and **as applied to claim 1 above**, Puleston, as modified by Murata, Puppa et al. and Storr, teach a system wherein a priority is set for a port to be switched, and a clock supply line priority table representing a priority for port switching for supplying the synchronous clock is prepared at each node ("... a router stores a routing table which includes information on which connections lead to particular groups of addresses, priorities for connections to be used, and rules for handling both routine and special cases of traffic." Paragraph [0003] Lines 6-10).

Conclusion

5. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street

Alexandria, VA 22314

Any inquiry concerning this communication or early communications from the Examiner should be directed to Salvador E. Rivas whose telephone number is (571) 270-1784. The examiner can normally be reached on Monday-Friday from 7:00AM to 3:30PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Huy D. Vu can be reached on (571) 272- 3155. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Salvador E. Rivas
S.E.R./ser

December 17, 2007

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